CLAIMS:

1. A method of identifying an inaccurate model of a hardware circuit comprising the steps of:

simulating the model of the circuit by applying a plurality of signals, said plurality of signals having at least one abstract data type level to provide a set of expected results;

replacing the or each abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model;

resimulating the model with said expanded set; and

comparing the two sets of results and providing an output signal indicating if the model is inaccurate if the results contradict.

2. A method as claimed in claim 1, wherein the model is an HDL model.

3. A method as claimed in claim 2, wherein said plurality of signals are selected from a standard logic package data set comprising one or more simple logic levels and one or more abstract data type levels.

4. A method according to claim 3 further comprising the step of, when said abstract data type is an X selected from the standard logic package, expanding each X into a 0 and a 1.

5. A method as claimed in claim 3, wherein the or each abstract signal is converted into two simple logic signals.

6. A method according to any preceding claim further comprising the steps of, during a process of verifying the accuracy of the model, said model being a digital model, comparing the results of the model with the results from the simulation of an analog model of the circuit, identifying whether the digital model is an accurate model and only comparing the digital model results with the analogue model

results if the digital model is determined in said comparing step to be accurate.

7. A method according to claim 6, in which said analog model is a SPICE model of the hardware test cell.

8. A method according to any preceding claim further comprising the steps of during simulation for the plurality of signals determining the value of each output from said model; and

during resimulation determining for the expanded set the value of each output from the model.

9. A method as claimed in any preceding claim wherein said model is a digital model.

10. A system for identifying an inaccurate model of a hardware circuit comprising:

means for simulating the model of the circuit by applying a plurality of signals, said plurality of signals having at least one abstract data type level to provide a set of expected results;

means for replacing the or each abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model;

means for resimulating the model with said expanded set;

means for comparing the two sets of results and providing an output signal indicating if the model is inaccurate if the results contradict.

11. A system as claimed in claim 9, wherein said system is a computer system.

12. A computer program comprising program code means for performing any of the steps of any of claims 1 to 9 when the program is run on a computer.